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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,558	02/09/2001	David James Hathaway	BUR920000137US1	1548

21254 7590 11/21/2003

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/780,558	Applicant(s) HATHAWAY ET AL.	
	Examiner Helen B Rossoshek	Art Unit 2825	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2, 9 are objected to because of the following informalities:

Claim 2 line 5 after "defects" make a space.

Claim 9 has antecedent basis issue.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Belkhale et al. ("Timing analysis with known false sub graphs ",Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 IEEE/ACM International Conference on , 5-9 Nov. 1995, Page(s): 736 –739).

As to claims 1, 2, 11, 13-19 Belkhale et al. teaches generating a composite graph comprising K+1 copies of an original graph, the original graph represents the network with defects and K is a predetermined maximum number of defects on any of the at least one path as shown on the Fig. 1 wherein G is original timing graph with false subgraphs (F_1 ... F_k) and k is a maximum number of false subgraphs (false path) (Page 736); and performing an analysis of the network using the composite graph (Page 736); adding a first type of defect edge for at least K of the delay edge E in the original timing graph, such that each first type of defect edge has a delay that reflects a timing behavior of the circuit in a presence of a first type of defect from the source node of E in $copy_i$ of the timing graph to the sink node of E in $copy_{i+1}$ of the composite timing graph, for all values of I such that 0<=I<=K; and for each node, calculating at least one parameter (Page 737); at least one arrival time (AT) of an input signal, at least one required arrival time (RAT) for the input signal, an at least one slack value for the input signal, wherein each the slack value is a difference between the at least one RAT and the at least one AT (Page 737); an apparatus for performing K-fault tolerant static timing analysis for a network composed of at least one path, each the path including at least two nodes, the apparatus comprising: a control unit; and a memory unit by using an IBM RS/6000 processor (Page 738).

As to claims 3-8, 10, 12 and 20-22 Belkhale et al. teaches the network is composed of a plurality of nodes and each of the at least one path interconnects at least two of the plurality of nodes as shown on the Fig. 1 wherein v_1, v_2, v_3 and so on are nodes of the network; and the performing static analysis further

comprises calculating, for each the node in each the path, at least one of the following: at least one arrival time (AT) of an input signal, at least one required arrival time (RAT) for the input signal, and at least one slack value for the input signal, wherein each the slack value is a difference between the at least one RAT and the at least one AT (Page 737); the defects are due to one or more of the following: manufacturing abnormalities insufficiently serious to cause a hard failure (Page 736); and voltage changes in floating components (Page 738); resulting in a single-fault analysis (K=1) (Page 737); for each I, where 0<=I<=K, a probability is associated with the condition of I defects in the path as shown on the Table 1, wherein the number of false per path (defects) starts from 0 (Page 738); the copies j, where 1<=j<=K, of the original timing graph include a preselected portion of the network preselected as being susceptible to defects (Page 736); the original timing graph includes only a preselected portion of the network preselected as being susceptible to defects which might be provided by user or detected automatically Page 736); the original timing graph includes at least one test edge between a pair of nodes, and where a copy of the test edge is inserted between the endpoints of the test edge in all pairs $copy_i$ and $copy_j$ of the original timing graph such that i+j=K within Definition 3 (Page 737); a defect test edge representing the behavior of the circuit in the presence of a first type of defect on the test edge, is inserted between the endpoints of the test edge in all pairs $copy_r$ and $copy_s$ of the original timing graph such that r+s+1=K within the Definition 4 (Page 737); a second type of defects edge is inserted between the source node of E in $copy_i$ of the timing graph to the sink node of E in $copy_{i+v}$ of

the composite timing graph, for all values of I such that 0<=I<=K-v and v>1, the second type of defect edge representing the behavior of the circuit in the presence of a second type of defect on edge E, the second type of defect being of lower probability than the first type of defect; and for each node, calculating at least one parameter (Page 738, Figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 703-305-3827. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HR

LEIGH M. GARBOWSKI
PRIMARY EXAMINER